REMARKS

In the Office Action[1], the Examiner took the following actions:

objected to the abstract;

objected to the specification for informalities;

objected to claims 3, 4, and 9 for informalities;

rejected claims 1, 2, and 9 under 35 U.S.C. § 103(a) as being unpatentable over Gavazzi AG (European Patent Application EP 0 723 166, "*Gavazzi*") in view of Ker et al. (U.S. Patent Application Publication No. 2002/0109153, "*Ker*");

rejected claims 3, 4, and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Gavazzi* and *Ker* in view of *Landt* (U.S. Patent No. 5,285,120);

rejected claims 5, 6, 11, and 12 under 35 U.S.C. § 103(a) as being unpatentable over *Gavazzi*, *Ker*, and *Landt*, in view of Enriquez et al. (U.S. Patent No. 6,950,514, "*Enriquez*");

rejected claim 7 under 35 U.S.C. § 103(a) as being unpatentable over *Gavazzi* and *Ker*, in view of *Fong* (U.S. Patent No. 6,005,439); and

rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over *Gavazzi* and *Ker*, in view of *Taylor* (U.S. Patent Application Publication No. 2002/0074988).

Applicant amends claims 1, 4, 6, 9, 10, and 11, cancels claim 3, and adds new claims 13-15. Accordingly, claims 1, 2, and 4-15 are pending and under current examination.

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicant declines to automatically subscribe to any statement or characterization in the Office Action.

Objection to the Abstract

In response to the objection to the Abstract, Applicant amends the Abstract in accordance with the Examiner's requirements. Therefore, Applicant respectfully requests the withdrawal of the objection to the Abstract.

Objection to the specification

In response to the various objections to the specification for informalities, Applicant amends the specification in accordance with the Examiner's requests. Therefore, Applicant respectfully requests the withdrawal of the objections to the specification.

Objections to claims 3, 4, and 9

Applicant respectfully traverses the objections to claims 3, 4, and 9 for informalities. Nevertheless, in order to further advance prosecution, Applicant amends claims 3 and 9 to recite "voltage" in place of "potential." Also, Applicant amends claim 4 to recite, in part, "wherein the first resistor and the first capacitor are components of a high pass filter that passes frequency elements of output signals. . .." Accordingly, Applicant respectfully requests the withdrawal of the objection to claims 3, 4, and 9.

Rejection of claims 1, 2, and 9 under 35 U.S.C. § 103(a)

Applicant respectfully traverses the rejection of claims 1, 2, and 9 under 35 U.S.C. § 103(a) as being unpatentable over *Gavazzi* in view of *Ker*. The key to supporting any rejection under 35 U.S.C. § 103 is the clear articulation of the reason(s)

why the claimed invention would have been obvious. Such an analysis should be made explicit and cannot be premised upon mere conclusory statements. MPEP § 2142, 8th Ed., Rev. 6 (Sept. 2007). "A conclusion of obviousness requires that the reference(s) relied upon be enabling in that it put the public in possession of the claimed invention." MPEP § 2145. Furthermore, "[t]he mere fact that references *can* be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art" at the time the invention was made. MPEP § 2143.01(III), internal citation omitted.

"[T]he framework for the objective analysis for determining obviousness under 35 U.S.C. § 103 is stated in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1996). . . . The factual inquiries . . . [include determining the scope and content of the prior art and] . . . [a]scertaining the differences between the claimed invention and the prior art." MPEP § 2141(II). "Office personnel must explain why the difference(s) between the prior art and the claimed invention would have been obvious to one of ordinary skill in the art." MPEP § 2141(III). In this application, a *prima facie* case of obviousness has not been established because the Office Action has neither properly determined the scope and content of the prior art nor properly ascertained the differences between the claimed invention and the prior art. Accordingly, the Office Action has failed to clearly articulate a reason why the prior art would have rendered the claimed invention obvious to one of ordinary skill in the art.

Here, a prima facie case of obviousness has not been established because the Examiner has neither properly determined the scope and content of the prior art nor properly ascertained the differences between the claimed invention and the prior art.

Accordingly, the Examiner has failed to clearly articulate a reason why the prior art would have rendered the claimed invention obvious to one of ordinary skill in the art.

Neither *Gavazzi* nor *Ker* discloses or suggests, at least, a capacitance detection circuit wherein "an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance; the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor" (emphasis added), as amended in independent claim 1. Applicant notes that claim 1, as amended, incorporates subject matter previously recited in claim 3.

In the rejection of claim 3, the Examiner first asserted that *Ker*, by showing a single input resistor "R" (Fig. 10) connected to the single junction between diodes D1, D2, D3, and D4 (Fig. 10), suggests both "the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor[,]" and "the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor." The Examiner cites *St. Regis Paper Co. v. Bemis Co.*, *193 USPQ 8*, in support of his allegation that "the use of a second resistor. . . constitutes duplication of parts," and that "mere duplication of essential working parts of a device involves only routine skill in the art." Office Action, p. 9.

In *St. Regis Paper Co.*, the court held that the plaintiff was not entitled to a patent to a particular bag ("Lokey bag") because the "method of strengthening a certain type of bag" by "putting one bag inside of another" is obvious (see legal.rights.com/F.2d/549/549.F2d.833.76-1044.html, p. 3). However, the court held that the plaintiff would have been entitled to a patent if "the fusion of the old elements . . created a synergistic combination." Id., p. 3. Claim 3 differs from the Lokey bag. That is, the use of a first and a second resistor, wherein "the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor" (claim 3), substantially differs from the principle of strengthening a certain bag by putting one bag inside of another. At the very least, claim 3 does not recite "duplicating" resistors to merely strengthen a resistance. Accordingly, the Examiner's application of *St. Regis Paper Co.* is improper.

The Examiner correctly conceded that *Gavazzi* and *Ker* fail to disclose "an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance" (claim 3). However, the Examiner used *Landt* to overcome this deficiency, alleging that "the use of a capacitor as a DC block, or to couple AC signals, is a common practice in the circuit design arts[.]" Office Action, p. 10). The Examiner further alleged that "a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of *Gavazzi* in view of *Ker* by employing well known or

conventional features such as a first and second capacitance between the output of the buffer amplifier and junction of the diodes, as disclosed by *Landt*, in order to block DC currents due to DC voltage offset in the buffer amplifier, and thereby prevent unwanted biasing (and capacitance due to varactor [sic] effects) of the diodes.)" (Office Action, p. 10). This is incorrect.

Landt merely teaches, in Col. 2, lines 30-32, "[t]he low-pass filter 20 on phase-shift channel 18 is separated from the input signal by capacitor 30 that acts as a dc block." While *Landt* teaches the function of capacitor 30 as a dc block, such teachings fails to teach or suggest a signal being outputted from a buffer amplifier to two RC high pass filters in parallel, which the "first capacitance," "second capacitance," "first resistor," and "second resistor," in claim 3 form. That is, *Landt* fails to teach or suggest that "an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance" (claim 3).

The Examiner also dismissed the "second capacitance" (claim 3) by alleging that it is a mere "duplication of parts," and is obvious in view of *St. Regis Paper Co.*. For at least the reasons discussed above in connection with the "second resistor" (claim 3), Applicant respectfully submits that the "second capacitance," as recited in claim 3, does not constitute mere duplication of capacitances.

Applicant further notes that a modern circuit rarely includes components that have never been used in another circuit. If each component in a novel circuit were able to be rendered obvious individually by a patchwork of prior art, no new circuit design

could ever be patented. Accordingly, Applicant respectfully reminds the Examiner that "[i]n determining the differences between the prior art and the claims, the question under 35 U.S.C. § 103 ***is not whether the differences themselves would have been obvious***, but ***whether the claimed invention as a whole would have been obvious***." MPEP § 2141.02(I), internal citations omitted (emphasis in original).

Since these differences between the prior art and claim 1 have not been addressed, no reason has been articulated why one of ordinary skill in the art would find claim 1 obvious. Therefore, a prima facie case of the obviousness of claim 1 has not been established over *Gavazzi*, *Ker*, and *Landt*. Claim 9, while of different scope, distinguishes from *Gavazzi*, *Ker*, and *Landt* for at least the same reasons as claim 1. Independent claims 1 and 9 are therefore allowable. Dependent claim 2 is also allowable at least by virtue of its dependence from independent claim 1. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 2, and 9 under 35 U.S.C. § 103(a).

Rejection of claims 3, 4, and 10 under 35 U.S.C. § 103(a)

Applicant respectfully traverses the rejection of claims 3, 4, and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Gavazzi* and *Ker* in view of *Landt*. Claims 3 and 4 depend from independent claim 1, and therefore incorporate each and every element of claim 1. As explained above, *Gavazzi*, *Ker*, and *Landt* fail to teach or suggest "an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance;

the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor," as recited in independent claim 1, and required by dependent claims 3 and 4.

Claim 10, while of different scope, is distinguishable from *Gavazzi*, *Ker*, and *Landt* for at least the same reasons as claim 1. That is, *Gavazzi*, *Ker*, and *Landt* fails to teach or suggest, at least, "a capacitor connected between an output terminal of the buffer amplifier unit and a first junction point of the first diode and the second diode; a resistor connected to the first junction point and to a point having voltage between voltage of the first power supply and voltage of the signal wire; a capacitor connected between the output terminal of the buffer amplifier unit and a second junction point of the third diode and the fourth diode; and a resistor connected to the second junction point and to a point having voltage between voltage of the second power supply and voltage of the signal wire," as recited in claim 10.

Because these differences between the prior art and claims 3, 4, and 10 have not been addressed, no reason has been articulated why one of ordinary skill in the art would find claims 3, 4, and 10 obvious. Therefore, a prima facie case of the obviousness of claims 3, 4, and 10 has not been established over *Gavazzi*, *Ker*, and *Landt*. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claims 3, 4, and 10 under 35 U.S.C. § 103(a).

Rejection of claims 5, 6, 11, and 12 under 35 U.S.C. § 103(a)

Applicant respectfully traverses the rejection of claims 5, 6, 11, and 12 under 35 U.S.C. § 103(a) as being unpatentable over *Gavazzi*, *Ker*, and *Landt*, in view of *Enriquez*. Claims 5 and 6 depend from independent claim 1, and therefore incorporate each and every element of claim 1. As explained above, *Gavazzi*, *Ker*, and *Landt* fails to teach or suggest "an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance; the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor," as recited in independent claim 1, and required by dependent claims 5 and 6.

Claim 11, while of different scope, is distinguishable from *Gavazzi*, *Ker*, and *Landt* for at least the same reasons as claim 1. That is, *Gavazzi*, *Ker*, and *Landt* fails to teach or suggest, at least, "a first capacitor and a second buffer amplifier unit connected in series between an output terminal of the first buffer amplifier unit and a first junction point of the first diode and the second diode; a first resistor connected to a junction point of the first capacitor and the second buffer amplifier unit and to a point having voltage between voltage of the first power supply and voltage of the signal wire; a second capacitor and a third buffer amplifier unit connected in series between the output terminal of the first buffer amplifier unit and a second junction point of the third diode and fourth diode; a second resistor connected to a junction point of the second

capacitor and the third buffer amplifier unit and to a point having voltage between voltage of the second power supply and voltage of the signal wire[,]" as recited in claim 11.

Enriquez fails to cure the deficiencies of *Gavazzi*, *Ker*, and *Landt*. *Enriquez* teaches a voltage reference filter for a subscriber line interface circuit including a buffer amplifier to the signal transport path though which one of the tip/ring signal currents is coupled to an input port of a sense amplifier. However, *Enriquez* is silent with respect to "a first capacitor and a second buffer amplifier unit connected in series between an output terminal of the first buffer amplifier unit and a first junction point of the first diode and the second diode; a first resistor connected to a junction point of the first capacitor and the second buffer amplifier unit and to a point having voltage between voltage of the first power supply and voltage of the signal wire; a second capacitor and a third buffer amplifier unit connected in series between the output terminal of the first buffer amplifier unit and a second junction point of the third diode and fourth diode; a second resistor connected to a junction point of the second capacitor and the third buffer amplifier unit and to a point having voltage between voltage of the second power supply and voltage of the signal wire[,]" as recited in claim 11.

Claim 12, while of different scope, is distinguishable from *Gavazzi*, *Ker*, and *Landt* for at least the same reasons as claim 1. That is, *Gavazzi*, *Ker*, and *Landt* fails to teach or suggest, at least, "canceling capacitance of the first diode and the third diode connected to the signal wire by connecting an output terminal of the buffer amplifier unit to a junction point of the first diode and the second diode via a first capacitance and to a junction point of the third diode and the fourth diode via a second capacitance; wherein

the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor[,]" as recited in claim 12.

Enriquez fails to cure the deficiencies of *Gavazzi*, *Ker*, and *Landt*. That is, *Enriquez* is silent with respect to "canceling capacitance of the first diode and the third diode connected to the signal wire by connecting an output terminal of the buffer amplifier unit to a junction point of the first diode and the second diode via a first capacitance and to a junction point of the third diode and the fourth diode via a second capacitance; wherein the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor[,]" as recited in claim 12.

Because these differences between the prior art and claims 5, 6, 11, and 12 have not been addressed, no reason has been articulated why one of ordinary skill in the art would find claims 5, 6, 11, and 12 obvious. Therefore, a prima facie case of the obviousness of claims 5, 6, 11, and 12 has not been established over *Gavazzi*, *Ker*, *Landt*, and *Enriquez*. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claims 5, 6, 11, and 12 under 35 U.S.C. § 103(a).

Rejection of claim 7 under 35 U.S.C. § 103(a)

Applicant respectfully traverses the rejection of claim 7 under 35 U.S.C. § 103(a) as being unpatentable over *Gavazzi* and *Ker*, in view of *Fong*. Claim 7 depends from independent claim 1, and therefore incorporates each and every element of claim 1. As explained above, *Gavazzi* and *Ker*, as well as *Landt*, fail to teach or suggest "an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance; the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor," as recited in independent claim 1, and required by dependent claim 7.

Fong fails to cure the deficiencies of *Gavazzi*, *Ker*, and *Landt*. *Fong* teaches a unity gain analog signal amplifier for low voltage applications including a MOSFET as an input circuit. However, *Fong* is silent with respect to "an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance; the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor," as recited in independent claim 1, and required by dependent claim 7.

Because these differences between the prior art and claim 7 have not been addressed, no reason has been articulated why one of ordinary skill in the art would find claim 7 obvious. Therefore, a prima facie case of the obviousness of claim 7 has not been established over *Gavazzi*, *Ker*, *Landt*, and *Fong*. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claim 7 under 35 U.S.C. § 103(a).

Rejection of claim 8 under 35 U.S.C. § 103(a)

Applicant respectfully traverses the rejection of claim 8 under 35 U.S.C. § 103(a) as being unpatentable over *Gavazzi* and *Ker*, in view of *Taylor*. Claim 8 depends from independent claim 1. As explained above, *Gavazzi* and *Ker*, as well as *Landt*, fail to teach or suggest "an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance; the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor," as recited in independent claim 1, and required by dependent claim 8.

Taylor fails to cure the deficiencies of *Gavazzi*, *Ker*, and *Landt*. *Taylor* teaches a method for determining the presence of voltage at capacitive test points and for determining the phase angle relationship between two capacitive points. However, *Taylor* is silent with respect to "an output terminal of the first buffer amplifier unit is

connected to a first junction point of the first diode and the second diode via a first capacitance, and to a second junction point of the third diode and the fourth diode via a second capacitance; the first junction point is connected to a point having voltage between voltage of the first power supply and voltage of the signal wire via a first resistor; and the second junction point is connected to a point having voltage between voltage of the second power supply and voltage of the signal wire via a second resistor," as recited in independent claim 1, and required by dependent claim 8.

Because these differences between the prior art and claim 8 have not been addressed, no reason has been articulated why one of ordinary skill in the art would find claim 8 obvious. Therefore, a prima facie case of the obviousness of claim 8 has not been established over *Gavazzi*, *Ker*, *Landt*, and *Taylor*. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claim 8 under 35 U.S.C. § 103(a).

New claims 13-15

New claims 13-15 depend from independent claim 1, and are allowable at least by virtue of their dependence from claim 1. Accordingly, Applicant respectfully requests that the Examiner allow claims 13-15.

Conclusion

In view of the foregoing, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
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Dated: December 4, 2008

By: /Jia W. Lu/
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Attachment: **Replacement Abstract**